Inventor: Marumoto
Docket No.: 12844.40US01
Title: IMAGE DISPLAY SYSTEM AND DISPLAY DEVICE
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Sheet 1 of 4

Fig. 1

a) Image processing IC
10 Camera
21 Camera I/F circuit
22 Buffer memory
23 Transfer address generating circuit
24 Area memory
25 Address converting circuit
26 Buffer memory control circuit
40 Work memory
60 Display panel

Fig. 2

a) Image processing IC
10 Camera
21 Camera I/F circuit
22 Buffer memory
23 Transfer address generating circuit
24 Area memory
25 Address converting circuit
26 Buffer memory control circuit
26A Area register control circuit
27 Area register
40 Work memory
60 Display panel

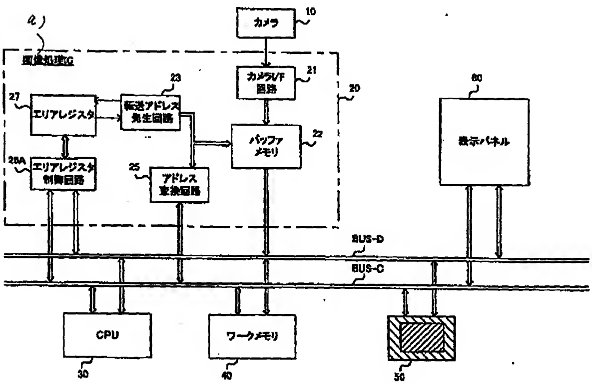

Fig. 3

a) Image processing IC
10 Camera
21 Camera I/F circuit
22 Buffer memory
23 Transfer address generating circuit
24 Area memory
25 Address converting circuit
26 Buffer memory control circuit
28 Read-out address generating circuit
29 Gate circuit
40 Work memory
60 Display panel

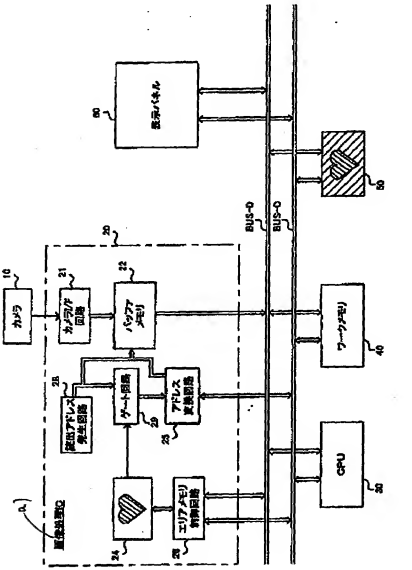

Fig. 4

a) Image processing IC
10 Camera
21 Camera I/F circuit
22 Buffer memory
23 Transfer address generating circuit
24 Area memory
25 Address converting circuit
26 Buffer memory control circuit
26B buffer memory control circuit
28 Read-out address generating circuit
29 Gate circuit
40 Work memory
60 Display panel